



WESTERN MICHIGAN UNIVERSITY
Manufacturing Research Center

*Temperature Measurement of the High
Pressure Phase Transformation (HPPT)
Region during the Micro-Laser Assisted
Machining (μ LAM) Process*

January 27th, 2012

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The Problem

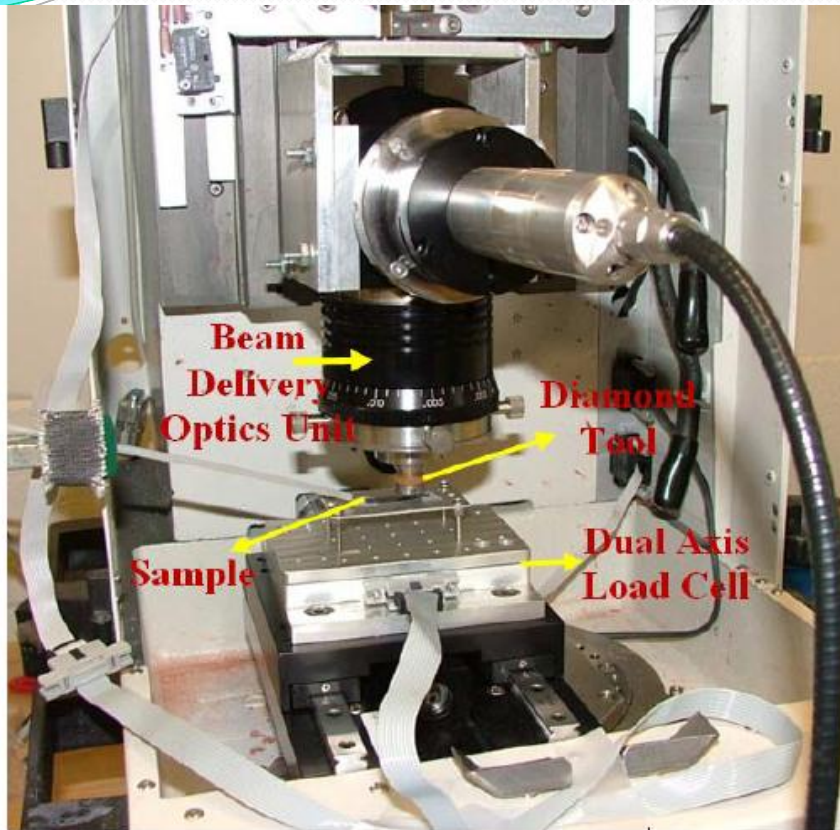


Figure 2: μ LAM system

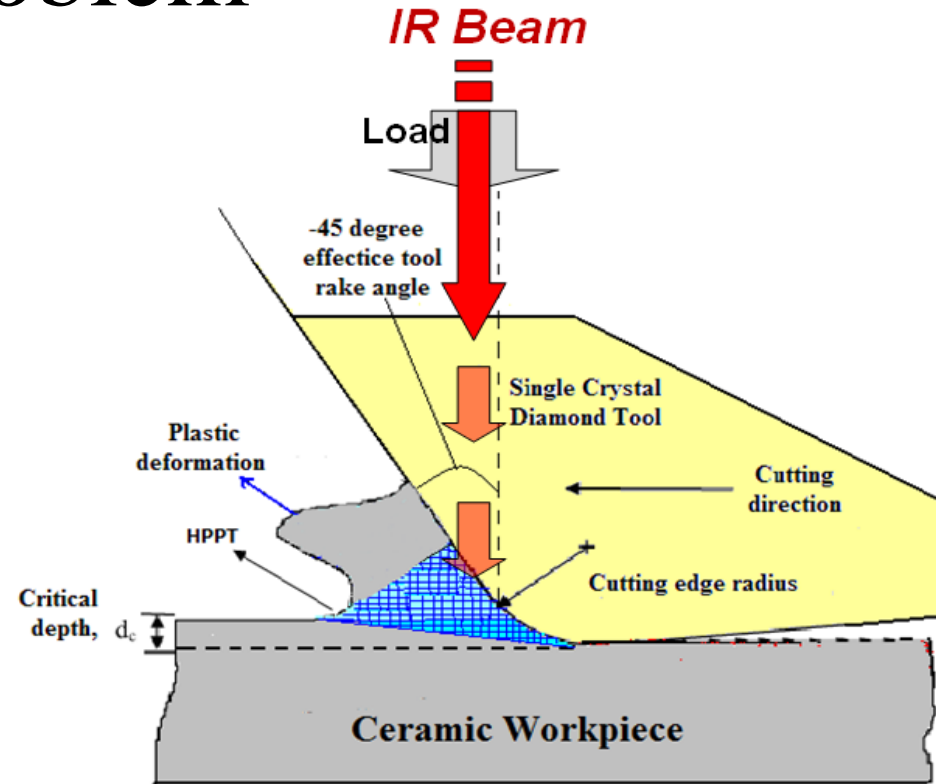
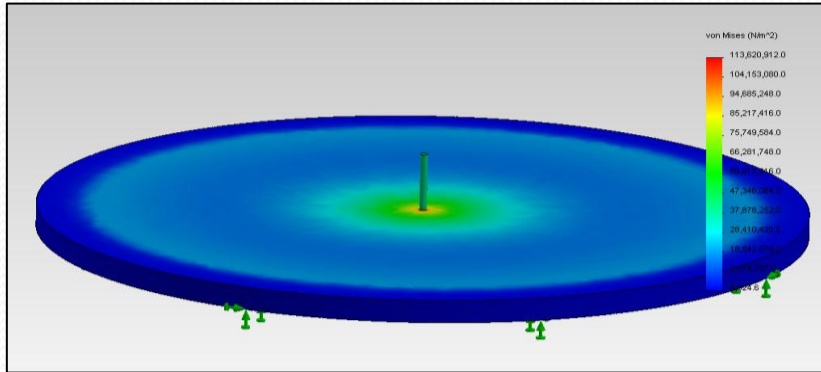


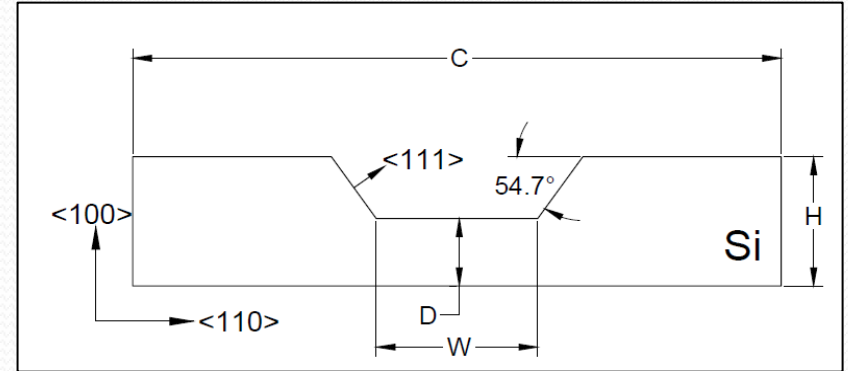
Figure 1: Schematic Cross-section of the micro-LAM system

- Micro-Laser Assisted Machining
- Machining Parameters \rightarrow Effectiveness of Micro-LAM
- Goal of the Project
- Challenge: Spot-size (50x50 microns), 500° C – 1500 °C, Not surface temperature

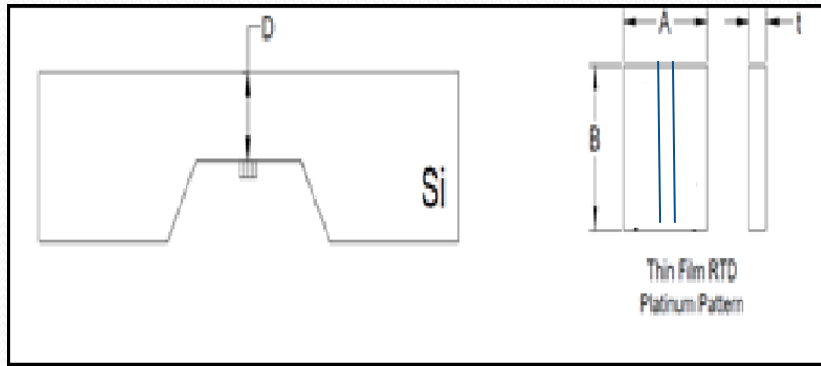
Proposed Solution



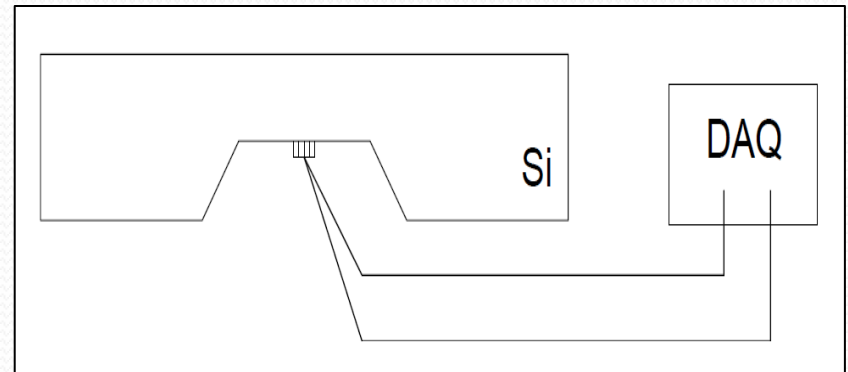
Step 1



Step 2








Step 3

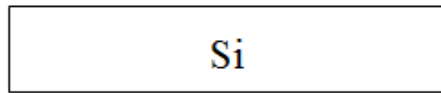


Step 4

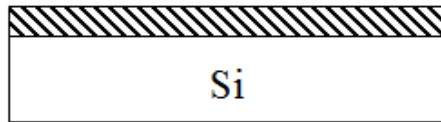
Step 5: FEA Thermal Model

Legend:

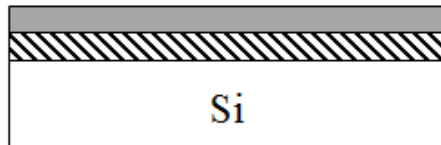
-  Silicon Wafer
-  SiO₂ Thin Film layer
-  Negative Photoresist
-  Quartz Plate for Mask
-  Chromium Thin Layer for Mask



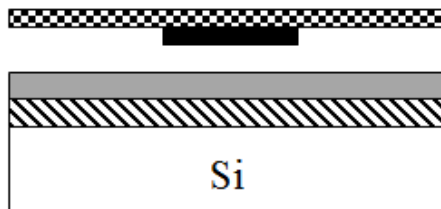
1. Clean the original 2-inch diameter Si wafer with a mixture of chemicals such as Sulfuric Acid and Hydrogen Peroxide to remove organic and inorganic contaminants that exist in the surface of the Si wafer. After applying the mixture of chemicals, apply distilled water to rinse the Si wafer.



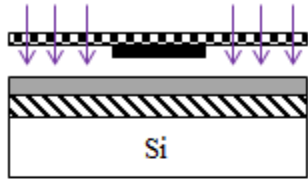
2. Oxidize the Si wafer with a SiO₂ thin film. This is accomplished by heating the Si substrate to temperatures around 900-1150°C.



3. A negative photoresist will be applied on top of the oxidized layer.



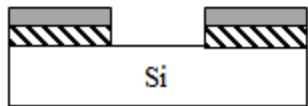
4. A mask is created with quartz plate (with an opaque pattern using a chromium layer) to pattern the width of the cavity side as shown in Figure 4. An estimated width "w" as shown in Figure 4 has been determined to be 5 mm.



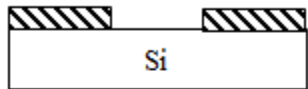
5. The photoresist is exposed to UV light with the fabricated mask in step 3. In this part, the chemical properties of the photoresist change making the unexposed part soluble to a developer.



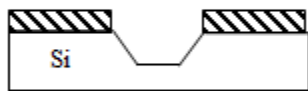
6. A developer solution is used to etch the unexposed photoresist.



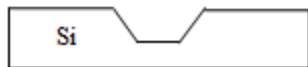
7. An etchant such as $\text{NH}_4\text{F} + \text{HF}$ is used to remove the oxide layer beneath the exposed photoresist (this attacks the oxide layer but not the exposed photoresist).



8. The exposed photoresist is removed by using H_2SO_4 (strong acid); this attacks the photoresist without causing damage to the Si or oxide layers.



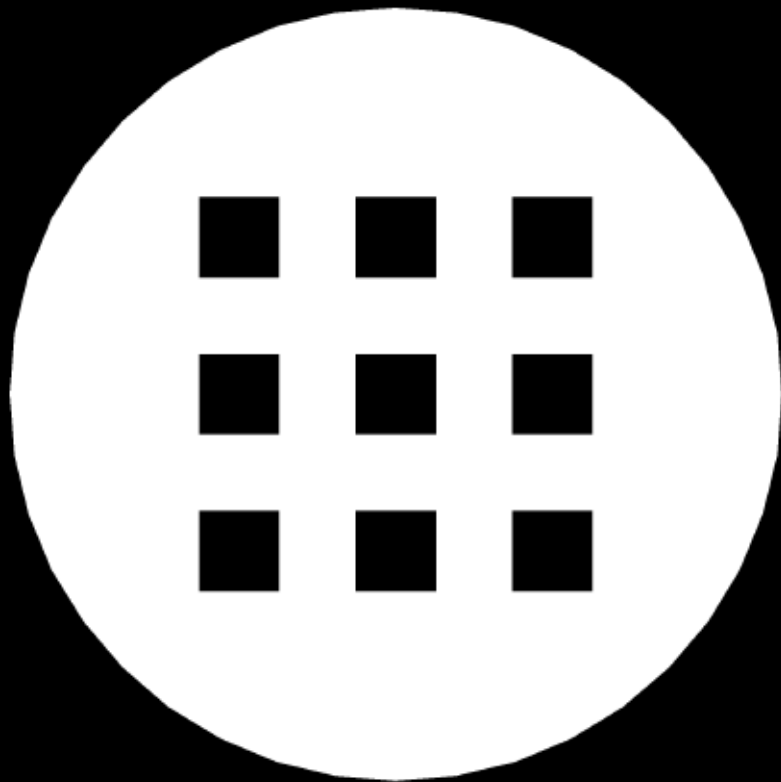
9. KOH is used to finally etch the Silicon (the concentration of the KOH solution used will determine the time that it needs to be applied according to etching rate tables such as that in Appendix c). This will result in a trapezoidal shape due to the different etching rates of Si in its different crystal faces exposed (The sloped side will make a 54.7° angle with the horizontal). Note that now the layer of SiO_2 layer works as an etch mask to only allow the wet anisotropic etch of Si in the oxide window.



10. The now exposed oxide layer is removed to expose the rest of the Si surface.



Figure 9: Three-dimensional View of the Etched Si (Silicon Microfabrication Techniques, 2007)



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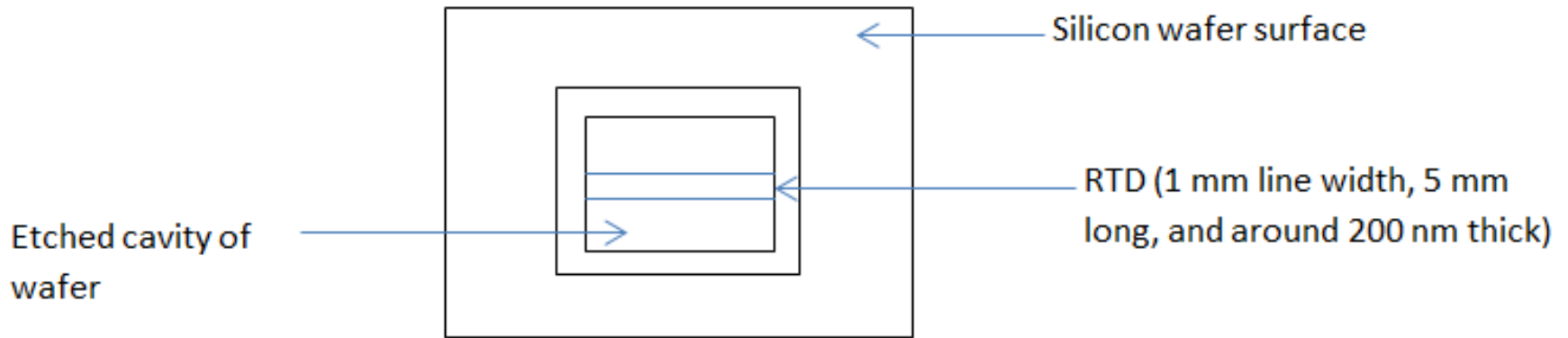
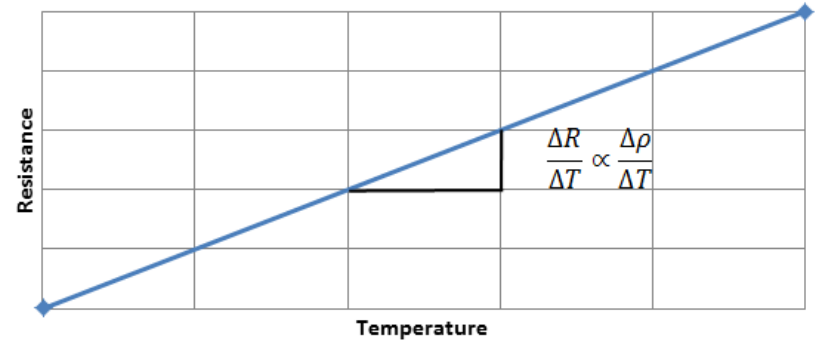


Figure 10: Bottom View of Etched Silicon with RTD across the Length of the Cavity Shown in Figure 9

$$R = \frac{\rho L}{A}$$

Conceptual Plot of RTDs' Change in Resistance with Temperature



RTD Construction Procedure

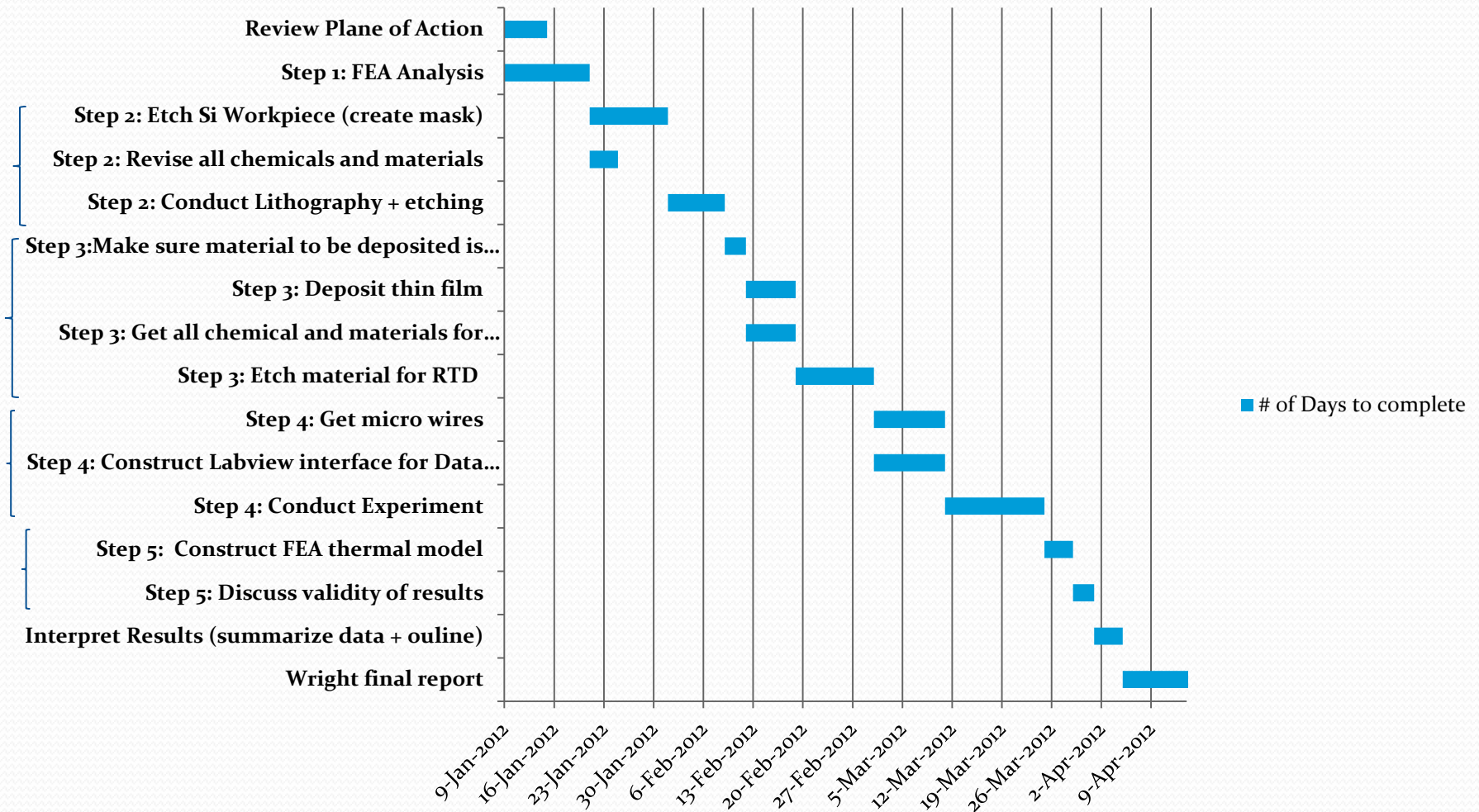
- 1. Adhesive layer** → Few nanometers
- 2. A thin layer of Platinum / Nickel** → 100-200 nm
- 3. A second mask**
- 4. A conventional lithography process as followed to etch**
- 5. Connect one micro wire** (20 to 50 microns)

Avoiding Error

- Stain measurement of RTD
- Avoid increasing the current level (self-conducting effect in RTD)

Schedule

Gantt Chart





Personnel

Student Members: *Jared McKinley & Dionisio Del Orbe*

Faculty Advisor:

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Dr. John Patten

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