1. **ECE 3550 Digital Design**

2. Credit Hours: 4 hours (3 – 3)

3. Coordinator: Dr. Janos L. Grantner, Professor of Electrical and Computer Engineering  
   Instructor in the Fall 2015 Semester: Dr. Janos L. Grantner  

4. Textbook(s) and/or Required Materials:  
   b. Materials disseminated using the ECE 3550 Class Web Page (the official media for the  
      class)  
   c. Nexys 4 FPGA Board along with the ECE 3550 Parts Kit  
   d. Current Xilinx Vivado WebPack along with the current Mentor Graphics ModelSim PE  
      Student Edition  

   Recommended Materials:  
   a. Instructor’s Lecture Notes, available on the ECE 3550 Class Web Page  

   References:  
   a. User’s Manuals and Data Sheets for the Nexys 4 Board and the Xilinx Artix-7 FPGA  
   b. Tutorials for the use of Vivado and ModelSim PE Student Edition, available on the  
      ECE 3550 Class Web Page  

5. Course information:  
   a. 2016-17 Catalog: Analysis of the real-time behavior of combinational and sequential  
      circuits. Analysis and synthesis of synchronous and asynchronous sequential logic  
      circuits. Systems level design of digital logic circuits using Programmable Logic  
      Devices.  
   b. Prerequisite: ECE 2500 with a grade of “C” or better.  
   c. Prerequisites by topic:  
      1. Introductory level digital logic design  
      2. Introductory knowledge of a PLD programming language  
   d. Required course in the Computer Engineering program  

6. Course Objectives: (ABET Learning Outcomes)  
   1. To provide experience to analyze, design, simulate and experimentally validate  
      combinational logic circuits using Programmable Logic Devices (FPGAs) (a, b, c, e)  
   2. To provide experience to analyze, design, simulate and experimentally validate system  
      control units based upon synchronous sequential circuits and using Programmable Logic  
      Devices (FPGAs) (a, b, c, e)  
   3. To provide experience to analyze, design, simulate and experimentally validate system  
      control units based upon asynchronous sequential circuits and using Programmable Logic  
      Devices (FPGAs) (a, b, c, e)  
   4. To provide experience to utilize contemporary circuit synthesis and simulation software  
      tools (k)  
   5. To develop skills to prepare effective written technical communications for engineering
analysis and design work through project reports (g)
6. To assess the students’ sense of ethical and professional responsibility (f)
7. To assess the students’ knowledge on contemporary issues (j).

7. Topics:
   a. Course overview, combinational logic design using VHDL, FPGAs, CPLDs and Xilinx and Mentor Graphics tools
   b. VHDL programming examples (combinational logic)
   c. Time faults in combinational logic circuits
   d. Stuck-at-faults in combinational logic
   e. Finite state machine (FSM) models
   f. Synchronous design with state machines, the ASM method
   g. VHDL programming examples (synchronous sequential circuits)
   h. Impediments to synchronous logic circuit design (clock skew and asynchronous inputs)
   i. Analysis and synthesis of asynchronous sequential machines, timing hazards in asynchronous circuits
   j. Design of asynchronous sequential machines with VHDL
   k. Introduction to microprocessor-based digital systems design
   l. Interfacing to intelligent I/O devices
   m. Microprogrammed system controllers

8. Design Projects:
   a. Design, build, and demonstration of the operation of a simple, synchronous, serial arithmetic unit (a bonus project is also offered). A report is required.
   b. Design, build, and demonstration of the operation of an synchronous, programmable, parallel I/O chip (a bonus project is also offered). A report is required.

9. Laboratory: 11 laboratory experiments
10. Evaluation:
    a. Examinations (50%)
    b. Design projects (20%)
    c. Laboratory(20%)
    d. Homework (10%)

11. Contribution to Professional Component:
    ABET professional component content as estimated by faculty member who prepared this course description:
    Engineering sciences: 2 credits or 50%
    Engineering design: 2 credits or 50%

**Prepared by: Dr. Janos L. Grantner**

**Date: March 20, 2016**